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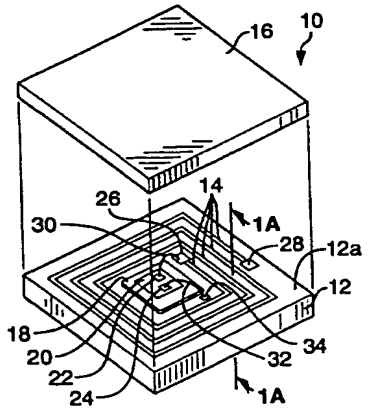
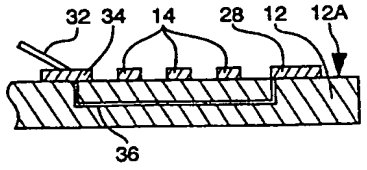
(54) Title: AN INTEGRATED CIRCUIT (IC) PACKAGE INCLUDING ACCOMPANYING IC CHIP AND COIL AND A METHOD OF PRODUCTION THEREFOR

(57) Abstract

An Integrated Circuit (IC) package is delineated comprising, in combination, a substrate layer, a coil located on a surface of the substrate layer, and an overmolded layer enclosing the surface. No conductor extends outside of the IC package. Preferably, the substrate layer comprises a Printed Circuit Board (PCB). Also, the IC package preferably comprises a single–side encapsulated IC package. The coil comprises an antenna preferably operating in the Radio Frequency (RF) range. The coil is mounted on the surface in a spiral pattern, generally following the shape of the perimeter of the surface of the substrate layer. The IC package further includes an IC chip mounted on the surface of the substrate layer and having a plurality of bonding pads. The IC chip may be located inside, outside, or on the spiral pattern. One or more underlying vias may be used wherein each is used to connect a bonding pad to an end of the coil. Preferably, the IC chip comprises an RF tag–type IC chip.





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AN INTEGRATED CIRCUIT (IC) PACKAGE INCLUDING ACCOMPANYING IC CHIP AND COIL AND A METHOD OF PRODUCTION THEREFOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention is in the field of Integrated Circuit (IC) packages and methods of production therefor and, more particularly, is an IC package having an accompanying IC chip and coil and a method of production therefor.

2. Description of the Related Art

The instant invention is associated with the general field of electrical engineering dealing with devices referred to as "tags" by those skilled in the art. In general terms, a tag includes a coil coupled to an IC chip in a package having no external conductors. A tag uses its coil, which functions as an antenna, to communicate with external devices using electromagnetic radiation penetrating and/or emanating from the tag. In the past, existing IC assemblies were used to create tags. More specifically, one would start with an IC lead frame. Then, using stamping or etching techniques, the lead frame was formed into a coil-like shape, thereby resulting in a pseudo-coil (i.e., the modified lead frame). Thereafter, the pseudo-coil was connected to an IC chip. Wire bonding was also required between the IC chip's bonding pads and the ends of the pseudo-coil; however, oftentimes due to the manner of construction of the tag, the wire leads would run over the pseudo-coil. Some time after wire bonding, the device had to be encapsulated on both the upper and lower areas of the device in order to fully

contain its internals.

There were several disadvantages associated with the above-described type of tag. First, there was no true coil; rather, a lead frame was modified through stamping processes, etching processes, or the like to form a pseudo-coil. Those skilled in the art realize that forming a "coil" (i.e., really a pseudo-coil) using one of these processes substantially increases the likelihood of damaging or destroying the lead frame, thereby slowing production and increasing costs. For the sake of clarity, note that a coil is a coil, a lead frame is a lead frame, and a lead frame modified to resemble a coil is, for the purposes of this disclosure, referred to as the "pseudo-coil." A second disadvantage results from the running of one or more of the bonding wires over the pseudo-coil. As a result, when the device is encapsulated, the bonding wires sometimes short out across the pseudo-coil's windings, thereby rendering the device useless. A third disadvantage results from the fact that the device begins with a lead frame and IC chip. More particularly, in order to fully encapsulate and physically isolate the device internals from the outside world, it is necessary to encapsulate or overmold both the upper and lower areas of the lead frame and IC chip combination. This raises construction costs, as it would be more cost effective to be able to fully encapsulate and physically isolate a tag with a single-side encapsulation of either the upper or lower areas of the device.

Therefore, there existed a need to provide an improved IC package which overcomes each of the aforementioned disadvantages, as well as offers additional benefits, and a method of production therefor.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an improved IC package and a method

of production therefor.

Another object of the present invention is to provide an improved tag and a method of production therefor.

Yet another object of the present invention is to provide an improved tag having a coil not made from a lead frame and a method of production therefor.

Another object of the present invention is to provide an improved tag having one or more underlying vias and a method of production therefor.

Still another object of the present invention is to provide an improved tag having a coil and an IC chip mounted on a substrate and a method of production therefor.

Another object of the present invention is to provide an improved tag which is fully isolated using single-side encapsulation and a method of production therefor.

BRIEF DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to one embodiment of the present invention, an Integrated Circuit (IC) package is disclosed comprising, in combination, a substrate layer, a coil located on a surface of the substrate layer, and an overmolded layer enclosing the surface. No conductor extends outside of the IC package (i.e., outside of the exterior of the IC package). Preferably, the substrate layer comprises a Printed Circuit Board (PCB) and the IC package comprises a single-side encapsulated IC package. Also, the coil preferably comprises an antenna operating in the Radio Frequency (RF) range. Typically, the coil is mounted on the surface in a spiral pattern which generally follows the shape of the perimeter of the surface of the substrate layer. Note however that the coil may be mounted on the surface in any pattern, either directly onto the surface or into an indentation therein. The IC package further includes an IC chip mounted on

the surface of the substrate layer and having a plurality of bonding pads. The IC chip may be located on a portion of the surface within a boundary formed by an innermost perimeter of the spiral pattern. Alternatively, the IC chip may be located above the spiral pattern, or on a portion of the surface outside a boundary formed by an outermost perimeter of the spiral pattern. A first conductor is provided between a first bonding pad of the plurality of bonding pads and a first end of the coil and a second conductor is provided between a second bonding pad of the plurality of bonding pads and the second end of the coil. The IC package further includes a first underlying via embedded in the substrate layer in substitution for the first conductor when placement of the IC chip on the surface would otherwise result in the first conductor extending over a portion of the coil, and a second underlying via embedded in the substrate layer in substitution for the second conductor when placement of the IC chip on the surface would otherwise result in the second conductor extending over a portion of the coil. Here, the phrase, "extending over a portion of the coil," means some portion of the coil other than one of its ends. Use of an underlying via generally implies the use of another bonding pad on the substrate surface for running a conductor from one of the IC chip's bonding pads. Preferably, the IC chip comprises an RF tag-type IC chip. Also, note that the IC package may comprise a double-side encapsulated IC package. Also, note that more than coil and more than one IC chip may be implemented in the instant invention.

According to another embodiment of the present invention, a method of producing an IC package is disclosed comprising the steps of providing a substrate layer, mounting an IC chip without a lead frame but having a plurality of bonding pads to a surface of the substrate layer, and mounting a coil to the surface of the substrate layer. Preferably, the substrate layer comprises a PCB. This method further comprises the step of overmolding the surface of the

substrate layer to provide a single-side encapsulated IC package having no conductor extending outside of the single-side encapsulated IC package. Alternatively, the method may include the additional step of overmolding an opposite surface of the substrate layer located opposite the aforementioned surface thereof to provide a double-side encapsulated IC package having no conductor extending outside of the double-side encapsulated IC package. Note that the coil comprises an antenna which preferably operates in the RF range. The coil is typically mounted on the surface in a spiral pattern that generally follows the shape of the perimeter of the surface of the substrate layer. Note however that the coil may be mounted on the surface in any pattern, either directly onto the surface or into an indentation therein. The IC chip may be located on a portion of the surface within a boundary formed by an innermost perimeter of the spiral pattern. Alternatively, the IC chip may be located above the spiral pattern, or on a portion of the surface outside a boundary formed by an outermost perimeter of the spiral pattern. This method further comprises the steps of connecting a first conductor between a first bonding pad of the plurality of bonding pads and a first end of the coil, and connecting a second conductor between a second bonding pad of the plurality of bonding pads and the second end of the coil. Additionally, the method comprises the steps of substituting a first underlying via embedded in the substrate layer for the first conductor when placement of the IC chip on the surface would otherwise result in the first conductor extending over a portion of the coil, and substituting a second underlying via embedded in the substrate layer for the second conductor when placement of the IC chip on the surface would otherwise result in the second conductor extending over a portion of the coil. Again, note that the phrase, "extending over a portion of the coil," means some portion of the coil other than one of its ends. Use of an underlying via generally implies the use of another bonding pad on the substrate surface for running a conductor from one of the IC chip's bonding

pads. Also, note that more than coil and more than one IC chip may be implemented in the instant invention. Lastly, note that the IC chip preferably comprises an RF tag-type IC chip.

The foregoing and other objects, features, and advantages of the invention will be apparent from the following, more particular, description of the preferred embodiments of the invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a simplified, exploded, perspective view of the IC package.

Fig. 1A is a cross-sectional view taken along the line 1A-1A of Figure 1 showing an underlying via.

Fig. 2 is a simplified, planar view of the top surface of the substrate layer of the IC package showing an alternative location for the package's IC chip.

Fig. 3 is a simplified, planar view of the top surface of the substrate layer of the IC package showing yet another location for the package's IC chip.

Fig. 4 is a perspective view showing the assembled IC package of Figure 1 in a single-side encapsulated arrangement.

Fig. 5 is a perspective view showing an assembled IC package in a double-side encapsulated arrangement.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 1, an Integrated Circuit (IC) package (hereafter more simply the "IC package" or "package") of the instant invention is shown and generally designated by reference number 10. Preferably, package 10 comprises, in combination, a substrate layer 12,

a coil 14 located on a surface 12a of the substrate layer 12, and an overmolded layer 16 enclosing the surface 12a. The package 10 has been generally defined as an IC package, which it most certainly can be; however, in the preferred embodiment, package 10 includes an RF tag-type IC chip. Those skilled in the art understand that an RF tag-type IC chip generally comprises an IC chip that communicates in the RF range with an external transmitter/receiver without the benefit of interconnecting conductors. Additionally, those skilled in the art recognize that tag-type IC chips that may operate outside of the RF range could be implemented into the instant invention. Note that no conductor extends outside of the package 10 (this can also be seen in Figures 4 and 5).

Still with reference to Figure 1, element 12 has been generally defined as the substrate layer 12; however, in the preferred embodiment, the substrate layer 12 comprises a Printed Circuit Board (PCB) 12. In the single-side encapsulated version of package 10, whether one implements a general substrate layer or a PCB 12 , no conductor or conductive portion protrudes from the surface thereof, other than surface 12a. For that reason, the singe-side encapsulated version (e.g., as seen in Figures 1-4) of package 10 has no conductors or conductive portions extending outside of the package 10. If the substrate layer 12 had one or more conductors or conductive portions protruding from a surface other than surface 12a, then the double-side encapsulation package 64 (see Figure 5) could be implemented. For example, in package 64 from Figure 5, there are one or more conductors or conductive portions on the surface of substrate layer 12 located opposite surface 12a, and they could make electrical contact with the outside world but for the inclusion of overmolded layer 66. In the preferred embodiment of the instant invention however, conductors or conductive portions rest only on surface 12a of substrate layer 12, so the single-side encapsulated version

of IC package 10 (see Figures 1 and 4) will suffice to keep all conductors or conductive portions contained within the package 10. Yet, Figure 5 points out that a double-side encapsulated version, which results in package 64, could be used with the instant invention, if required, to isolate all of the package's internal conductors or conductive portions from making physical contact with anything outside of package 64.

Still referring to Figure 1, the coil 14 preferably comprises an antenna 14, and if the package 10 operates in the RF range (i.e., if the tag-type IC chip 20 of package 10 operates in the RF range), then so does coil or antenna 14. Those skilled in the art realize that a coil, like coil 14, in a tag functions essentially as an antenna. The coil 14 is shown mounted on the surface 12a in a spiral pattern, which generally follows the shape of the perimeter of the surface 12a of the substrate layer 12. Preferably, the surface 12a of substrate layer 12 will be provided with a coil trace (not visible because the coil 14 is resting in it), indented into surface 12a for the coil 14 to rest. Additionally, surface 12a will have a die attach paddle 18 (i.e., an indentation into surface 12a) for an IC chip 20 to be mounted with an adhesive. Note that the IC chip 20 has a plurality of bonding pads 22 and 24. Those skilled in the art realize that bonding pads 22 and 24 are connected to portions of the IC chip 20 (not shown for clarity of the drawing) which permit operability of package 10. Preferably, the IC chip 20 comprises an RF tag-type IC chip. For the sake of clarity, an RF tag-type IC package, like package 10 in its preferred embodiment, includes an RF tag-type IC chip, like IC chip 20. The coil 14 is shown provided with bonding pads 26 and 28 at its ends., A conductor 30 connects bonding pad 22 from the IC chip 20 to one end of coil 14 via bonding pad 26. Another conductor 32 connects bonding pad 24 from the IC chip 20 to another bonding pad 34, which is connected using an underlying conductive via 36 to bonding pad 28 coupled to the other end of coil 14

(see Figure 1A).

Referring to Figure 1A, one sees that the underlying via 36 connects bonding pads 34 and 28. Those skilled in the art recognize that substrate layer or PCB 12 can be provided with the underlying via 36 as shown. Use of underlying via 36 prevents the possibility of shorting out coil 14 with a conductor (not shown) which would, but for the implementation of the underlying via 36, connect bonding pad 24 from the IC chip 20 to bonding pad 28 of the coil 14. The shorting which could possibly occur, but for the use of the underlying via 36, results from the overmolded layer 16 being encapsulated over surface 12a, thereby potentially pushing the aforementioned conductor (not shown) against one or more of the coil windings. Referring to Figure 1, note that the conductor 30 is used between bonding pads 22 and 26 because there is virtually no way for it to short out across the coil 14. However, a conductor (not shown) directly between bonding pads 24 and 28 would very likely short out across coil 14 when the package 10 was encapsulated. Thus, it is considered within the scope of the instant invention that whenever a conductor would have to run over the coil 14 in order to connect a bonding pad (e.g., 24) of the IC chip 20 with a bonding pad (e.g., 28) or even just the end of coil 14, then an underlying via like 36 would be used to obviate the potential shorting problem. This aim of the instant invention is intended to apply regardless of the location of IC chip 20 in relation to coil 14. For example as seen in Figure 1, when the IC chip 20 is located on a portion of the surface 12a within a boundary formed by an innermost perimeter of the coil's spiral pattern, the underlying via 36 (see Figure 1A) accomplishes the goal of avoiding any potential shorting across the coil 14.

Alternatively, in Figure 2, the IC chip 20 is located on a portion of the surface 12a outside a boundary formed by an outermost perimeter of the coil's spiral pattern. Here again,

use of an underlying via (not shown) precludes any shorting across coil 14. Like the embodiment of the package 10 shown in Figure 1, the package 10 in Figure 2 has a substrate layer or PCB 12 with a surface 12a. The surface 12a has an etched pattern (not shown) forming a generally spiral-shape to contain coil 14. A die attach paddle 18 is formed into surface 12a for the IC chip 20 to rest upon outside the boundary formed by the outermost perimeter of the coil's spiral pattern. One of the IC chip's bonding pads 46 is connected to one of the coil's ends via bonding pad 50 and conductor 48. Here, the conductor 48 has no potential to short out across the coil 14, and therefore, no underlying via is required. However, running a conductor (not shown) between IC chip bonding pad 38 and coil bonding pad 44 would have the potential of shorting across the coil 14, so an underlying via (not shown) is used. In particular, the IC chip's bonding pad 38 is connected to a bonding pad 42 via conductor 40, which has no possibility of shorting across coil 14. Then, bonding pad 42 would be coupled to bonding pad 44 using an underlying via, like that shown in Figure 1A, thereby avoiding any potential shorting problem in this embodiment of the package 10. Note that the package 10 here would, like those shown in Figures 4 and 5, have either single or double encapsulation, as required.

Referring to Figure 3, the package 10 has its IC chip 20 located above the coil's spiral pattern. Again, there would be a substrate layer or PCB 12 having a surface 12a with an etched pattern to accommodate coil 14. Here, as elsewhere, the pattern shown is generally spiral shaped; however, those skilled in the art realize that it is within the scope of the instant invention to lay out coil 14 into an indented pattern on surface 12a having some other shape. For example, the spiral pattern may not have edges as shown (i.e., the pattern may be rounded or curved). The IC chip 20 would have to be connected to the surface 12a and coil 14 using a

non-conductive adhesive material well known to those skilled in the art in order to isolate the IC chip 20 from the coil 14 except for desired end connections hereafter described. In particular, one of the IC chip's bonding pads 58 would be connected to one end of the coil 14 via a bonding pad 62 and conductor 60. Another bonding pad 52 of the IC chip 20 would be connected to the other end of coil 14 via bonding pad 56 and conductor 54. In this embodiment of package 10, there is very little possibility of either conductor 60 or conductor 54 shorting out across coil 14, so no underlying via is used. However, to further ensure against the possibility of shorting across coil 14 by either conductor 60 or conductor 54, one could use one or two underling vias analogous to that shown in Figure 1A. Again, note that the package 10 here would, like those shown in Figures 4 and 5, have either single or double encapsulation, as required.

Referring to Figures 4 and 5, note that any of the aforementioned embodiments of the package 10 could be implemented using either single-side encapsulation (as shown in Figure 4) or double-side encapsulation (as shown in Figure 5). If the substrate layer or PCB 12 had exposed conductors or circuitry only on surface 12a, then typically single-side encapsulation with overmolded layer 16 would be used. Double-side encapsulation would not be required, or desired from a cost standpoint, in this case since single-side encapsulation with overmolded layer 16 would fully isolate the package's internals from the outside world (other than electromagnetic radiation penetrating package 10 for use as a tag). On the other hand, if a substrate layer or PCB 12 had conductors or circuitry exposed not only on surface 12a, but also on an additional surface (e.g., on a surface opposite surface 12a), then double-side encapsulation would be required to isolate the package 10. Here, one would use overmolded layers 16 and 66 over substrate layer or PCB 12 to form the fully isolated package 64. Here

again, the internals of package 64 would be accessible to electromagnetic radiation, as desired for tag operation.

OPERATION

Initially, one must be provided with an appropriate substrate layer or PCB material 12. What is "appropriate" depends on the number of coils 14 and IC chips 20 used, as well as their relative placement, and whether one or more sides of the substrate layer or PCB 12 has exposed conductors or circuitry. For the purposes of discussion, assume the case of a single coil 14 and a single IC chip 20 wherein only surface 12a of substrate layer or PCB 12 has exposed conductors or circuitry. In this case, the substrate layer or PCB 12 will have an indented pattern for accommodating coil 14, and an indented die attach paddle for accommodating the IC chip 20. Also, depending on the location of the IC chip 20 relative to the coil 14, there may be one or more underlying vias in the substrate layer or PCB 12. Again for the purpose of discussion, assume the case shown in Figures 1 and 1A, so a single underling via 36 would be provided with the substrate layer or PCB 12.

The coil 14 can be either specially fabricated and then adhered into its indented pattern in surface 12a, or the coil 14 can be deposited into its indented pattern using an evaporative process well known to those skilled in the art. Note again that the indented pattern for coil 14 could take any one of a number of different shapes; however, for the purposes of discussion, assume the shape shown in Figure 1. In order to attach the IC chip 20 to surface 12a, an adhesive would be applied to the indented die attach paddle area, then the IC chip 20 would typically be heat cured into place. Note that a non-conductive adhesive may be required if, for example, the IC chip 20 were placed over the coil 14 (e.g., see Figure

3). Appropriate conductors (e.g., 30 and 32 in Figure 1) would then be wire bonded into place. This arrangement takes advantage of the underlying via 36 (see Figure 1A). Lastly, the substrate layer or PCB 12 would be encapsulated, in a manner well known to those skilled in the art, using overmolded layer 16 to form package 10. Those skilled in the art realize that regardless of whether one or more coils 14 or IC chips 20 are used, whether single or double-side encapsulation is used, and regardless of the relative position of the coil(s) 14 to the IC chip(s) 20, this general approach, or a slightly modified version thereof, could be followed to produce packages 10 or 64 (see Figures 4 and 5). Thereafter, the finished package 10 or 64 operates in a manner well known to those skilled in the art of tag operation.

Although the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that changes in form and detail may be made therein without departing from the spirit and scope of the invention. For example, as opposed to using a single coil 14 per package 10 as shown here, one could envision a similar package 10 using more than one coil 14, in which case one or more IC chips 20 could be located anywhere on surface 12a, and one or more underlying vias (like 36 in Figure 1A) could be used.

CLAIMS

1. An Integrated Circuit (IC) package comprising, in combination:

a substrate layer;

a coil located on a surface of said substrate layer; and

an overmolded layer enclosing said surface.

2. The IC package of Claim 1 wherein no conductor extends outside of said IC package.

3. The IC package of Claim 1 wherein said substrate layer comprises a Printed Circuit Board (PCB).

4. The IC package of Claim 1 wherein said IC package comprises a single-side encapsulated IC package.

5. The IC package of Claim 1 wherein said coil comprises an antenna.

6. The IC package of Claim 5 wherein said antenna operates in the Radio Frequency (RF) range.

7. The IC package of Claim 1 wherein said coil is mounted on said surface in a spiral pattern.

8. The IC package of Claim 7 wherein said spiral pattern generally follows the shape of the perimeter of said surface of said substrate layer.

9. The IC package of Claim 7 further including an IC chip mounted on said surface of said substrate layer and having a plurality of bonding pads.

10. The IC package of Claim 9 wherein said IC chip is located on a portion of said surface within a boundary formed by an innermost perimeter of said spiral pattern.

11. The IC package of Claim 9 wherein said IC chip is located above said spiral pattern.

12. The IC package of Claim 9 wherein said IC chip is located on a portion of said surface outside a boundary formed by an outermost perimeter of said spiral pattern.

13. The IC package of Claim 9 wherein a first conductor is provided between a first bonding pad of said plurality of bonding pads and a first end of said coil and wherein a second conductor is provided between a second bonding pad of said plurality of bonding pads and the second end of said coil.

14. The IC package of Claim 9 further including an underlying via embedded in said substrate layer and having a single connection to said coil comprising a connection from a coil end of said underlying via to one of a first end and a second end of said coil, and wherein said underlying via is connected to one bonding pad of said plurality of bonding pads at the other end of said underlying via.

15. The IC package of Claim 13 further including a first underlying via embedded in said substrate layer in substitution for said first conductor when placement of said IC chip on said surface would otherwise result in said first conductor extending over a portion of said coil, and a second underlying via embedded in said substrate layer in substitution for said second conductor when placement of said IC chip on said surface would otherwise result in said second conductor extending over a portion of said coil.

16. The IC package of Claim 9 wherein said IC chip comprises an RF tag-type IC chip.

17. The IC package of Claim 1 wherein said IC package comprises a double-side encapsulated IC package.

18. A method of producing an Integrated Circuit (IC) package comprising the steps of:

providing a substrate layer;

mounting an IC chip without a lead frame but having a plurality of bonding pads to a surface of said substrate layer; and

mounting a coil to said surface of said substrate layer.

19. The method of Claim 18 wherein said substrate layer comprises a Printed Circuit Board (PCB).

20. The method Claim 18 further comprising the step of overmolding said surface of said substrate layer to provide a single-side encapsulated IC package having no conductor extending outside of said single-side encapsulated IC package.

21. The method of Claim 20 further comprising the step of overmolding an opposite surface of said substrate layer located opposite said surface thereof to provide a double-side encapsulated IC package having no conductor extending outside of said double-side encapsulated IC package.

22. The method of Claim 18 wherein said coil comprises an antenna.

23. The method of Claim 22 wherein said antenna operates in the Radio Frequency (RF) range.

24. The method of Claim 18 wherein said coil is mounted on said surface in a spiral pattern.

25. The method of Claim 24 wherein said spiral pattern generally follows the shape of the perimeter of said surface of said substrate layer.

26. The method of Claim 24 wherein said IC chip is located on a portion of said surface within a boundary formed by an innermost perimeter of said spiral pattern.

27. The method of Claim 24 wherein said IC chip is located above said spiral pattern.

28. The method of Claim 24 wherein said IC chip is located on a portion of said surface outside a boundary formed by an outermost perimeter of said spiral pattern.

29. The method of Claim 18 further comprising the steps of:

connecting a first conductor between a first bonding pad of said plurality of bonding pads and a first end of said coil; and

connecting a second conductor between a second bonding pad of said plurality of bonding pads and the second end of said coil.

30. The method of Claim 18 further comprising the steps of:

providing an underlying via embedded in said substrate layer and having a single connection to said coil comprising a connection from a coil end of said underlying via to one of a first end and a second end of said coil; and

connecting the other end of said underlying via to one bonding pad of said plurality of bonding pads.

31. The method of Claim 29 further comprising the steps of:

substituting a first underlying via embedded in said substrate layer for said first conductor when placement of said IC chip on said surface would otherwise result in said first conductor extending over a portion of said coil; and

substituting a second underlying via embedded in said substrate layer for said second conductor when placement of said IC chip on said surface would otherwise result in said second conductor extending over a portion of said coil.

32. The method of Claim 18 wherein said IC chip comprises an RF tag-type IC chip.

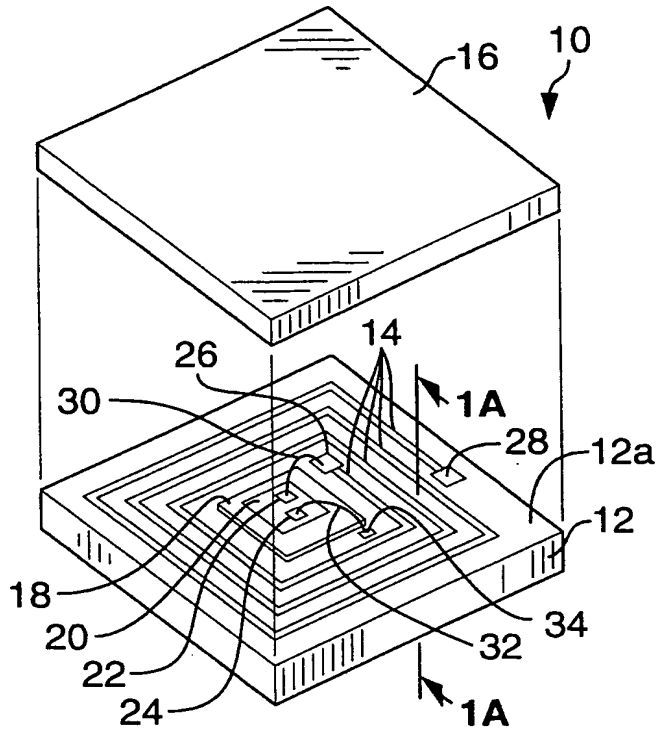

Figure 1

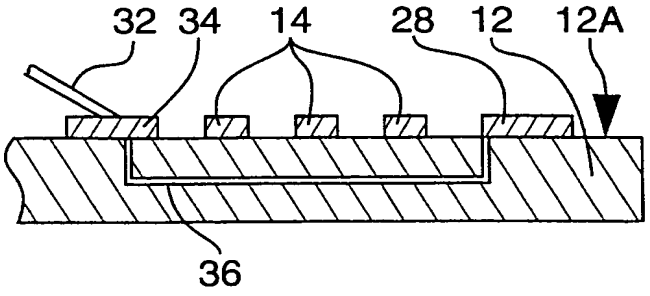

Figure 1A

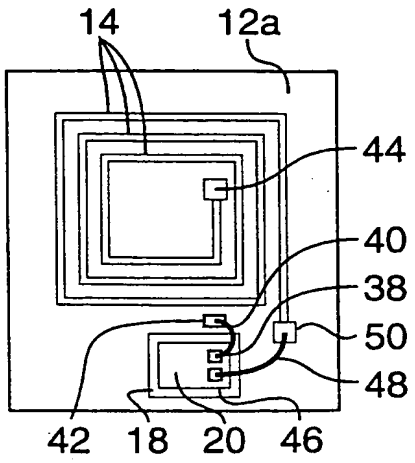

Figure 2

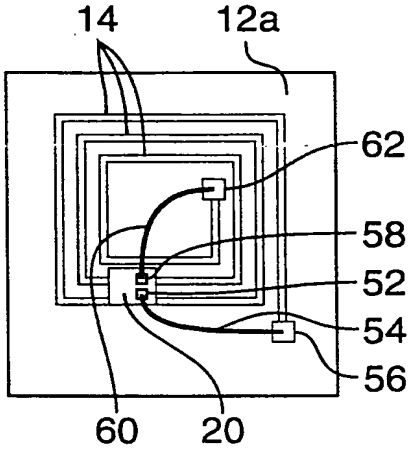

Figure 3

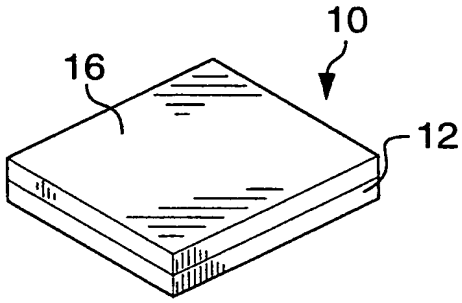

Figure 4

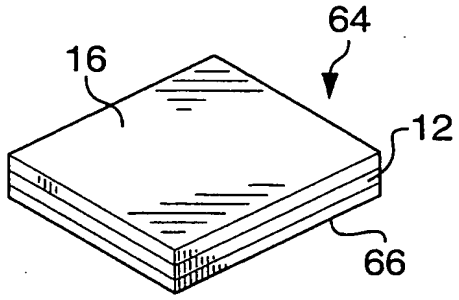

Figure 5

INTERNATIONAL SEARCH REPORT

I. national Application No
PCT/US 99/00438

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/64

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L G06K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 095, no. 010, 30 November 1995 -& JP 07 176646 A (TOSHIBA CORP), 14 July 1995 see abstract -& US 5 710 458 A (KAUSHIKI KAISHA TOSHIBA) 20 January 1998 see the whole document ---	1-10, 13-16, 18-20, 22-26, 29-32
X	FR 2 675 930 A (MITSUBISHI ELECTRIC CORP) 30 October 1992 see the whole document --- -/--	1-3, 5-10,13, 17-19, 21-26,29

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 April 1999	29/04/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Zeisler, P

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INTERNATIONAL SEARCH REPORT

:national Application No
PCT/US 99/00438

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	WO 97 26621 A (LEDUC MICHEL ;MARTIN PHILIPPE (FR); GEMPLUS CARD INT (FR); KALINOW) 24 July 1997 see page 7, line 6 - page 826; figures 4D,4E,5B see page 12, line 12 - page 14, line 10 see page 15, line 13 - line 24	1-3, 5-11,13, 16,18, 19, 22-27, 29,32
X	PATENT ABSTRACTS OF JAPAN vol. 097, no. 005, 30 May 1997 -& JP 09 001970 A (HITACHI CHEM CO LTD), 7 January 1997 see abstract	1-3,5-7, 9,12,13, 18,19, 22-24, 28,29
X	EP 0 692 770 A (GEMPLUS CARD INT) 17 January 1996 see page 2, column 2, line 46 - page 3, column 4, line 2; figures 1,3	1-10, 18-20, 22-26,29
X	EP 0 786 357 A (ROHM CO LTD) 30 July 1997 see page 4, column 6, line 23 - page 5, column 7, line 9; figures 1-3,15	1-10,12, 13, 18-20, 22-26, 28,29

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Information on patent family members

national Application No
PCT/US 99/00438

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